# POWER MODES

## ADC Power ON

**PON\_CTL.**

* PON\_LS\_ADC\_ATB1/2: 1

**PVT\_REF\_GEN\_BIST\_1**

* ENA\_ADC\_ATB1/2: 1

## ADC Power Off

**PON\_CTL**

* PON\_LS\_ADC\_ATB1/2: 0

**PVT\_REF\_GEN\_BIST\_1**

* ENA\_ADC\_ATB1/2: X (doesn’t matter)

*OR*

**PON\_CTL**

* PON\_LS\_ADC\_ATB1/2: 1

**PVT\_REF\_GEN\_BIST\_1**

* ENA\_ADC\_ATB1/2: 0

To clarify preferred way after a startup (i.e. outside of calibration and FuSa timeslot)

## ADC Sleep mode

**PON\_CTL**

* PON\_LS\_ADC\_ATB1/2: 1

**PVT\_REF\_GEN\_BIST\_1**

* ENA\_ADC\_ATB1/2: 1

**ADC\_CTL\_FUNC:**

* ADC1/2\_CONT\_MONO 0
* *(Basically, switch off the clock, if the ADC was sampling in continuous mode before. Not relevant for Mono mode)*

Potential use for calibration:

1. Power ON the ATB ADC at the beginning of calibration sequence.
2. (into) Sleep mode in between calibration items
3. Power OFF at the end of calibration sequence

# Default values for all ATB ADC modes:

*The values below are already set as default in register map. No need to configure initially (to be confirmed)*

**ADC1\_CTRL\_1/2:**

* SET\_LDO\_VREFP: 011 [trim value from OTP]
* SET\_LDO\_VDDA: 100 [trim value from OTP]
* SET\_LDO\_BIAS\_VREFP: 01010 [trim value from OTP]
* SET\_LDO\_BIAS\_VDDA: 01010 [trim value from OTP]

**ADC1/2\_TEST:**

* DEBUG\_SPEED: 001

**ADC1/2\_CTRL\_0:**

* DIV2\_CAL: 10000 [trim value from OTP]

# Operational differential input mode

**ADC1/2\_CTRL\_0:**

* SEL\_SE\_CONV: 0 [trim value from OTP]
* SEL\_DIV2: 0 [trim value from OTP].

## Analog input selection (see diagrams below)

### **vp\_adc** *(positive Atb output)* **-> vin[0] -> DACp** *(positive input of ADC)*

### **vn\_adc** *(negative Atb output)* **-> vin[1] -> DACn** *(negative input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 10
* SEL\_ADC1/2\_MUX\_VN 10

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 0X

### **vp\_adc** *(positive Atb output)* **-> vin[3] -> DACn** *(negative input of ADC)*

### **vn\_adc** *(negative Atb output)* **-> vin[2] -> DACp** *(positive input of ADC)*

*(swapping p- and n- signals)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 00
* SEL\_ADC1/2\_MUX\_VN 00

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 1X

### 

# Operational single-ended input mode

**ADC1/2\_CTRL\_0:**

* SEL\_SE\_CONV: 1 [trim value from OTP]
* SEL\_DIV2: 0 [trim value from OTP].

## Analog input selection (see diagram below). Opposite ATB output (VP/N\_ADC) as VNEG\_SE. *Using the ground of IP. Question: what is the advantage of using VSSA\_1V8 – ground of ATB at all?*

### **vp\_adc** *(positive Atb output)* **-> vin[0] -> DACp** *(positive input of ADC)*

### **vn\_adc** *(negative Atb output)* **-> vneg\_se -> DACn** *(negative input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 10
* SEL\_ADC1/2\_MUX\_VN 01
* SEL\_ADC1\_VNEG\_SE 01

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 00

### **vp\_adc** *(positive Atb output)* **-> vin[3] -> DACn** *(negative input of ADC)*

### **vn\_adc** *(negative Atb output)* **-> vneg\_se\* -> DACp** *(positive input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 00
* SEL\_ADC1/2\_MUX\_VN 01
* SEL\_ADC1\_VNEG\_SE 01

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 11

### **vn\_adc** *(negative Atb output)* **-> vin[2] -> DACp** *(positive input of ADC)*

### **vp\_adc** *(positive Atb output)* **-> vneg\_se\* -> DACn** *(negative input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 01
* SEL\_ADC1/2\_MUX\_VN 00
* SEL\_ADC1\_VNEG\_SE 10

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 10

### **vn\_adc** *(negative Atb output)* **-> vin[1] -> DACn** *(negative input of ADC)*

### **vp\_adc** *(positive Atb output)* **-> vneg\_se\* -> DACp** *(positive input of ADC)*

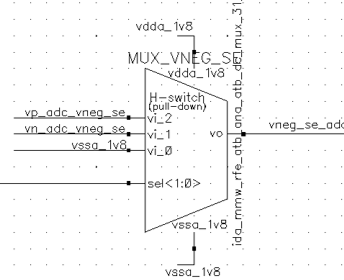
**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 01
* SEL\_ADC1/2\_MUX\_VN ~~11~~ 10
* SEL\_ADC1\_VNEG\_SE 10

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 01





## Analog input selection (see diagram below). VSSA\_1V8 as VNEG\_SE

### **vp\_adc** *(positive Atb output)* **-> vin[0] -> DACp** *(positive input of ADC)*

### **vssa\_1V8 -> vneg\_se -> DACn** *(negative input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 10
* SEL\_ADC1/2\_MUX\_VN XX
* SEL\_ADC1\_VNEG\_SE 00

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 00

### **vp\_adc** *(positive Atb output)* **-> vin[3] -> DACn** *(negative input of ADC)*

### **vssa\_1V8 -> vneg\_se\* -> DACp** *(positive input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP 10
* SEL\_ADC1/2\_MUX\_VN XX
* SEL\_ADC1\_VNEG\_SE 00

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 11

### **vn\_adc** *(negative Atb output)* **-> vin[2] -> DACp** *(positive input of ADC)*

### **vssa\_1V8 -> vneg\_se\* -> DACn** *(negative input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP XX
* SEL\_ADC1/2\_MUX\_VN 00
* SEL\_ADC1\_VNEG\_SE 00

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 10

### **vn\_adc** *(negative Atb output)* **-> vin[1] -> DACn** *(negative input of ADC)*

### **vssa\_1V8 -> vneg\_se\* -> DACp** *(positive input of ADC)*

**ATB\_DC\_SWITCHES:**

* SEL\_ADC1/2\_MUX\_VP XX
* SEL\_ADC1/2\_MUX\_VN ~~11~~ 10
* SEL\_ADC1\_VNEG\_SE 00

**ADC1/2\_CTRL\_0:**

* SEL\_IN: 01

# If external node is measured, internal atb select set to 0

**ATB\_CTL1 :**

* ATB1\_SEL: 00000000
* ATB2\_SEL: 00000000